

Ferroelectric La-Sr-Co-O/Pb-Zr-Ti-O/La-Sr-Co-O heterostructures on silicon via template growth

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Citation: *Applied Physics Letters* **63**, 3592 (1993); doi: 10.1063/1.110106

View online: <http://dx.doi.org/10.1063/1.110106>

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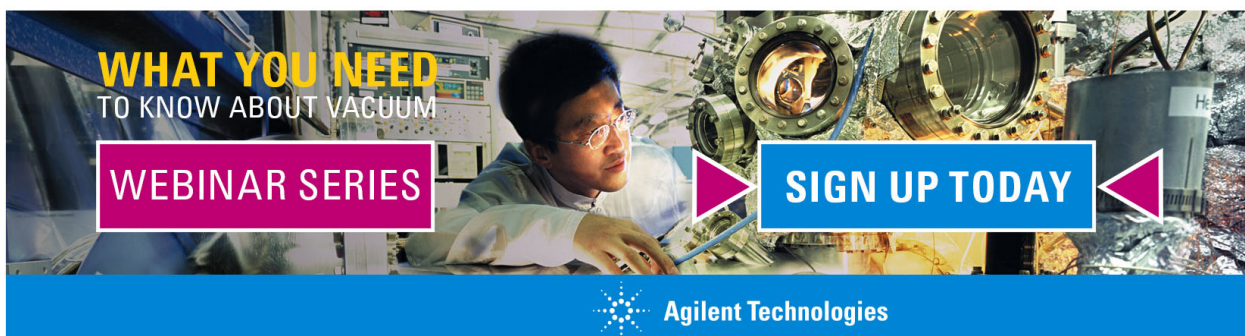
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Ferroelectric La-Sr-Co-O/Pb-Zr-Ti-O/La-Sr-Co-O heterostructures on silicon via template growth

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(Received 13 November 1992; accepted for publication 13 October 1993)

Ferroelectric $\text{Pb}_{0.9}\text{La}_{0.1}\text{Zr}_{0.2}\text{Ti}_{0.8}\text{O}_3$ thin film capacitors with a symmetrical La-Sr-Co-O top and bottom electrodes have been grown on [001] Si with yttria stabilized zirconia (YSZ) buffer layer. A layered perovskite "template" layer (200–300 Å thick), grown between the YSZ buffer layer and the bottom La-Sr-Co-O electrode, is critical for obtaining the required orientation of the subsequent layers. When compared to the capacitors grown with the Y-Ba-Cu-O top and bottom electrodes, these structures possess two advantages: (i) the growth temperatures are lower by 60–150 °C; (ii) the capacitors show a larger remnant polarization ΔP (ΔP =switched polarization–nonswitched polarization), 25–30 $\mu\text{C}/\text{cm}^2$, for an applied voltage of only 2 V (applied field of 70 kV/cm). The fatigue, retention, and aging characteristics of these new structures are excellent.

Ferroelectric thin film materials have had a strong resurgence in research and development recently, primarily because of their potential use as nonvolatile, random access memories integrated with existing Si complimentary metal-oxide-semiconductor (CMOS) transistor circuitry.^{1–4} Conventionally the ferroelectric thin films, such as lead zirconate titanate (PZT), are deposited onto Pt-coated Si wafers with Pt top contact electrodes to form the capacitor structure. Thin film deposition techniques including sol-gel spin-on sputtering, chemical vapor deposition, and pulsed laser deposition are being used to deposit the thin films. Solutions to reliability issues such as fatigue, aging, retention, and imprinting are being explored concurrently with issues related to integration with CMOS drive circuitry.^{5–10}

Recent studies have shown that metal oxide electrodes yield capacitors with better fatigue properties compared to conventionally used Pt electrodes.^{11–13} Specifically, it has been demonstrated that the superconducting cuprates such as Y-Ba-Cu-O (YBCO), which are metallic at room temperatures, can be used as top and bottom electrodes. The capacitors so formed show very little bipolar fatigue.¹³ The YBCO top and bottom electrodes in these capacitors are typically grown in the temperature regime of 700–800 °C, which is higher than that conventionally used in Si process technology (about 550 °C). In an effort to reduce the growth temperature, we have been studying a variety of other metallic perovskite compounds as potential candidates for the top and bottom electrodes. Among such oxides, the cubic perovskite La-Sr-Co-O (LSCO) has been shown to have desirable metallic properties (room temperature resistivity as low as 90 $\mu\Omega\text{ cm}$) in recent studies wherein the thin film heterostructures were grown on single crystalline oxide substrates (SrTiO_3).^{11,12} Even though LSCO is metallic and has good structural compatibility with the SrTiO_3 substrates used, in order to be useful in integrated ferroelectric memories, they have to be grown on Si wafers. We have taken the approach of finding methods to grow these epitaxial capacitor structures on Si using

structural templates and chemical barrier layers to alleviate the problem of the chemical and structural incompatibility.

The capacitor structures are grown by pulsed excimer laser deposition onto [001] Si which is buffered with an yttria stabilized zirconia (YSZ) surface layer. The important feature of this approach is that it can be carried out at a substrate heater temperature of 640 °C (the substrate temperature is approximately 50 °C lower), which is substantially lower than the previously reported range of 700–800 °C for YBCO top and bottom electrodes.¹³ The details of the deposition conditions are similar to those reported for the capacitors with YBCO top and bottom electrodes. Direct deposition of the LSCO/PLZT/LSCO layer onto the YSZ buffer layer yielded a [110] oriented film as evidenced by the x-ray diffraction pattern in Fig. 1(a). Capacitors fabricated from this heterostructure were only weakly ferroelectric (see Fig. 2). We attribute the strong [110] orientation to the large difference in lattice parameters between YSZ (5.16 Å) and LSCO (3.82 Å), which is detrimental for a simple cube-on-cube orientation relationship. This problem was overcome through the use of a very thin (approximately 200–300 Å) layer of *c*-axis oriented $\text{Bi}_4\text{Ti}_3\text{O}_{12}$, which is not conducting and acts as a perovskite "template" layer. This template layer is also grown at the same growth temperature. Due to its strong structural anisotropy, $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ grows in the *c*-axis orientation and provides a surface that is suitable for the growth of the subsequent LSCO and PLZT layers. The LSCO top and bottom electrodes were 1000 Å thick while the PLZT layer was 2700 Å thick. With such a template layer, the LSCO/PLZT/LSCO heterostructure is *c*-axis oriented, as illustrated in the x-ray diffraction pattern in Fig. 1(b). In addition to the 001 Bragg peaks for the LSCO and PLZT layers, the [0 0 14] Bragg peak of the bismuth titanate layer is also observed. Note also that both the (002)PLZT and the (200)PLZT peaks are observed, indicating that a certain fraction of the PLZT has the *c*-axis in-plane. X-ray

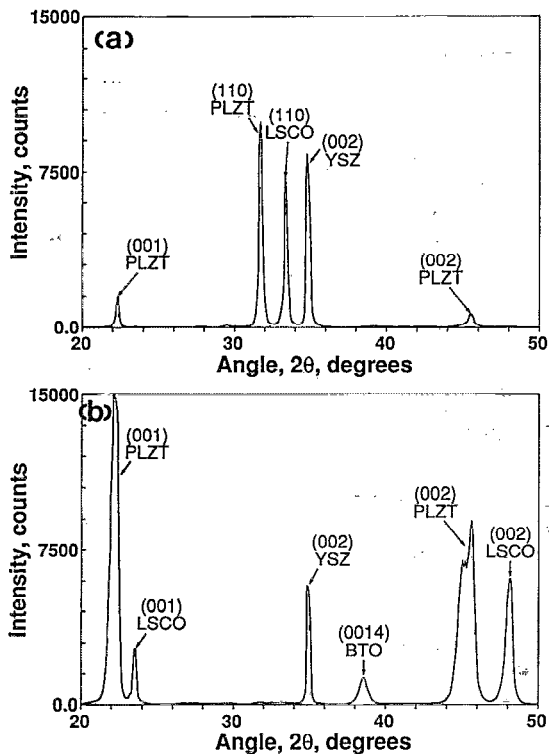


FIG. 1. X-ray diffraction patterns from the LSCO/PLZT/LSCO capacitor structures grown on [001] Si with a YSZ buffer layer; (a) without the bismuth titanate "template" layer; and (b) with the bismuth titanate template layer.

rocking curves about the 001 Bragg peak of the PLZT layer yielded a full width at half-maximum of 0.7° – 0.8° . Rutherford backscattering analyses confirmed the composition of the various layers to be commensurate with that of the target and no lead loss was observed as long as the substrate heater temperature was kept below 650°C . Test capacitors were fabricated using a shadow mask with areas

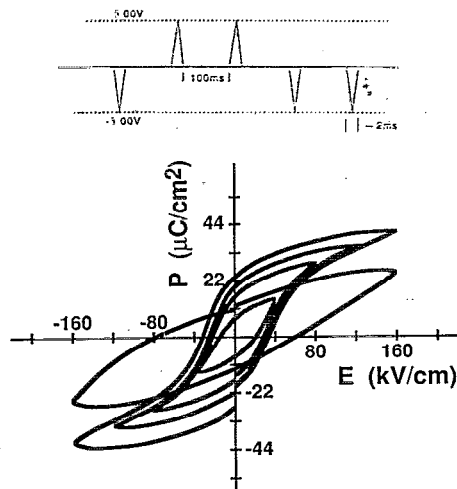


FIG. 2. A family of pulsed hysteresis loops for the test capacitors grown on top of the bismuth titanate template layer. Also shown is the leaky dielectric loop for the capacitor structure grown without the template layer.

in the range of 2×10^{-5} – 10^{-4} cm^2 . Electrical measurements were made using the Radiant Technologies tester, RT66A, in conjunction with a pulse generator. Pulsed polarization and hysteresis measurements were carried out using the sequence of pulses shown in the inset to Fig. 2. For the bipolar fatigue experiments, internally generated $8.65 \mu\text{s}$ -wide square pulses or externally generated square pulses were used. After the end of each fatigue period, the polarization characteristics of the capacitors were measured using the same pulse sequence shown in the inset to Fig. 2.

Figure 2 shows a family of pulsed hysteresis loops obtained from the test capacitors at applied voltages ranging from 2 to 4 V. Also shown in this figure is the "hysteresis loop" from the [110] oriented heterostructure that was grown without the bismuth titanate template layer. It can be seen that without the template layer, the hysteresis loop has the appearance of that from a leaky dielectric, rather than a ferroelectric material. However, the [001] oriented films grown on the bismuth titanate template show clear ferroelectric hysteresis loops. The coercive fields are in the range of 25–35 kV/cm, corresponding to coercive voltages of 0.6–0.8 V. Pulse polarization measurements show that the structures have remnant polarizations (defined as $\Delta P = \text{switched polarization} - \text{nonswitched polarization}$, both being measured at the bottom of the pulse) in the range of 8 – $35 \mu\text{C}/\text{cm}^2$ (depending upon the applied voltage). For example, for an applied voltage of 2 V, the remnant polarization is measured to be in the range of 21 – $25 \mu\text{C}/\text{cm}^2$. These values are much larger than those obtained before with YBCO top and bottom electrodes (at the same voltage).¹³

Bipolar fatigue over a range of test frequencies, logic state retention, and aging experiments were carried out on these capacitors to study their reliability characteristics. These experiments were performed on capacitors with the smallest area, to minimize the RC time constant. Figure 3 shows the results of the bipolar fatigue experiments at two frequencies, 40 kHz and 1 MHz, both at $\pm 2 \text{ V}$. The $\pm \Delta P$ values (ΔP is as defined in the previous paragraph) are plotted in this figure as a function of fatiguing time for the two frequencies. For example, at 1 MHz there is an approximately 10%–15% loss of remnant polarization after 10^{12} bipolar cycles. Fatigue testing at higher voltages, i.e., 5 V, yielded a similar behavior as a function of fatigue cycles. Pulse polarization studies after the fatigue experiment show that this loss of polarization is reversible by poling for longer times at the cycling voltage. This fatigue behavior is consistent with earlier results from test capacitors with Y-Ba-Cu-O top and bottom electrodes, as well as those with RuO_2 electrodes.^{11–13} The exact reasons for the superior fatigue characteristics of capacitors with metallic oxide top and bottom electrodes as compared to Pt electrodes are not clear. We attribute the better performance to the nature of the electrode-ferroelectric interface and not to phenomena occurring in the bulk. Evidence in support of this interpretation is the fact that when the top LSCO is replaced by a Pt electrode, the hysteresis loops are strongly displaced toward the positive field direction and more im-

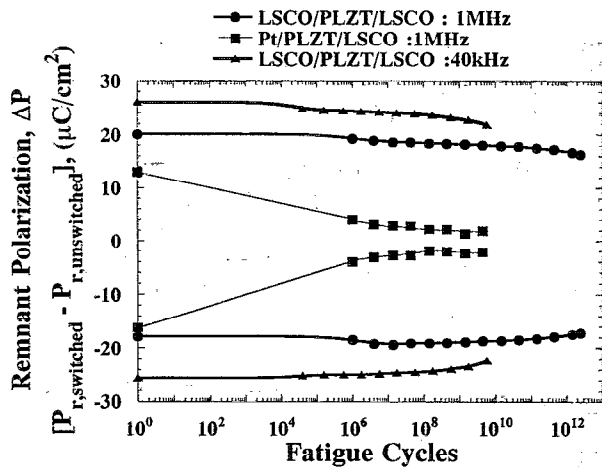


FIG. 3. A plot of remnant polarization ΔP (ΔP = switched remnant polarization - nonswitched remnant polarization) vs time for bipolar fatigue at 2 V and frequencies of 40 kHz and 1 MHz for the LSCO/PLZT/LSCO capacitor grown using the bismuth titanate template layer. Also shown is the fatigue data for a capacitor structure in which the bottom electrode is LSCO and the top is Pt. Note that this capacitor fatigues rapidly.

portantly, they fatigue dramatically, as shown in Fig. 3. These results are also consistent with what was observed in the case of Y-Ba-Cu-O electrodes.¹³

We then studied the logic state retention and discrimination after fatiguing for 10^{12} cycles. The retention experiments were typically carried out using a write voltage of ± 2 V, with a pulse width of 8.6 μ s. The read pulse is 2 ms wide and is of variable amplitude (typically 1.5–2 V). The

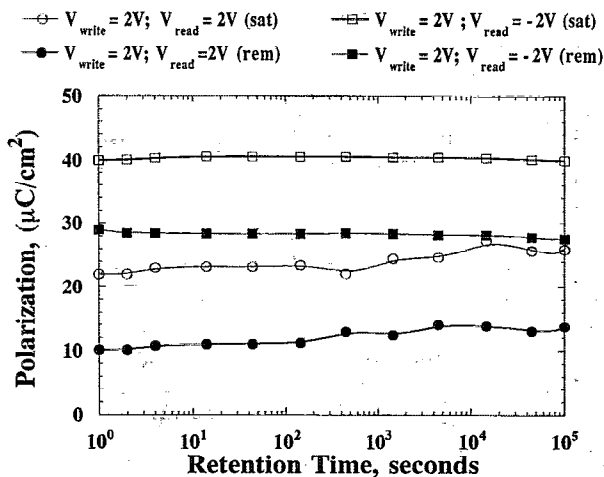


FIG. 4. Logic state retention for the LSCO/PLZT/LSCO capacitor after fatiguing for 10^{12} cycles. The write voltages are ± 2 V and the read voltage is 2 V. The capacitor shows sufficient distinction ($\sim 13 \mu\text{C}/\text{cm}^2$) between these two states. Open marks correspond to polarization values in the saturation condition and filled marks correspond to polarization values in the remnant condition.

polarization values at the top (i.e., at the maximum read voltage) and at the bottom (i.e., when the read voltage is zero) of the read pulse are measured. Figure 4 shows the results of this experiment, carried out over five decades of time. Polarization values for both the logic state “1” (write/read pulses of opposite polarity) and the logic “0” (write/read pulses of the same polarity) are plotted in this figure. Under these test conditions, we find that there is more than a sufficient difference (~ 10 – $12 \mu\text{C}/\text{cm}^2$) in polarization values between the two states. For read voltages of 1.5 V, the difference in polarization values for the two states is smaller (9 – $10 \mu\text{C}/\text{cm}^2$) but it is consistently maintained for the five decades of time. Pulsed hysteresis loops and polarization measured before and after the retention test for both logic states show no difference in shape and magnitude. We are presently studying the effect of the write and read pulse width on the long-term retention characteristics and imprinting effects.

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